



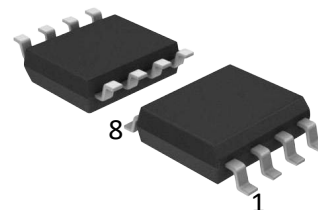
# PJM204A5DPPA

## Dual P-Enhancement Field Effect Transistor

### Features

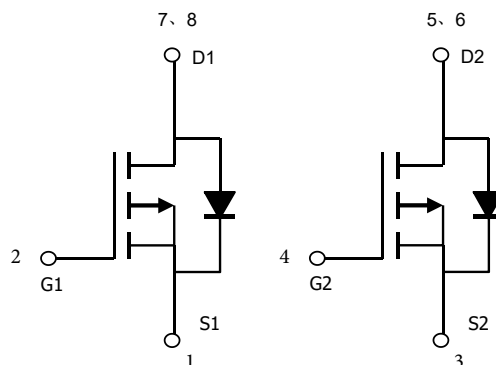
- Dual P-channel MOSFET
- Super high dense cell design
- Rugged and reliable
- $V_{DS}=-20V$ ,  $I_D=-4.5A$   
 $R_{DS(on)}=65m\Omega(Max)@V_{GS}=-10V$

SOP-8



### Application

- Power management in laptops
- Portable equipment
- Battery powered systems.



### Absolute Maximum Ratings

Ratings at 25°C ambient temperature unless otherwise specified.

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>Note 1</sup>	$I_D$	-4.5	A
Pulsed Drain Current <sup>Note 1</sup>	$I_{DM}$	-20	A
Diode Continuous Forward Current <sup>Note 1</sup>	$I_S$	-2.0	A
Total Power Dissipation <sup>Note 1</sup> (Single Operation)	$T_A=25^\circ C$	2	W
	$T_A=100^\circ C$	0.8	
Operating Junction Temperature	$T_J$	150	$^\circ C$
Storage Temperature	$T_{STG}$	- 55 to + 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Value	Units
Maximum Junction-to-Ambient <sup>Note 1</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$

Note:1. Surface Mounted on 1 in.<sup>2</sup> pad area,  $t \leq 10sec.$



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### Electrical Characteristics

Ratings at 25°C ambient temperature unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
<b>Static Characteristics</b>							
Drain-to-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = 0\text{ V}, I_D = -250\mu\text{A}$	-20	-	-	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	$T_A = 25^\circ\text{C}$	-	-	-1	uA
			$T_J = 85^\circ\text{C}$			-10	
Gate-to-source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-0.55	-0.8	-1.4	V	
Drain-to-source On-resistance <sup>Note 1</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}$	-	52	65	mΩ	
		$V_{GS} = -4.5\text{ V}, I_D = -3.5\text{ A}$	-	68	78		
		$V_{GS} = -2.5\text{ V}, I_D = -2.2\text{ A}$	-	88	98		
<b>Dynamic Characteristics</b> <sup>Note 2</sup>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -6\text{ V}$	-	415	-	pF	
Output Capacitance	$C_{oss}$		-	223	-		
Reverse Transfer Capacitance	$C_{rss}$		-	84	-		
Total Gate Charge	$Q_g$	$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -2.7\text{ A}$	-	5.8	-	nC	
Gate-Source Charge	$Q_{gs}$		-	0.85	-		
Gate-Drain Charge	$Q_{gd}$		-	1.7	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, I_D = -1.0\text{ A}, R_{GEN} = 6\Omega, V_{GEN} = -10\text{ V}$	-	13	25	ns	
Turn-On Rise Time	$t_r$		-	36	60		
Turn-Off Delay Time	$t_{d(off)}$		-	42	70		
Turn-Off Fall Time	$t_f$		-	34	60		
<b>Source-Drain Diode characteristics</b>							
Body Diode Voltage <sup>Note 1</sup>	$V_{SD}$	$I_S = -1.0\text{ A}, V_{GS} = 0\text{ V}$		-0.7	-1.3	V	

Note: 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2 %.

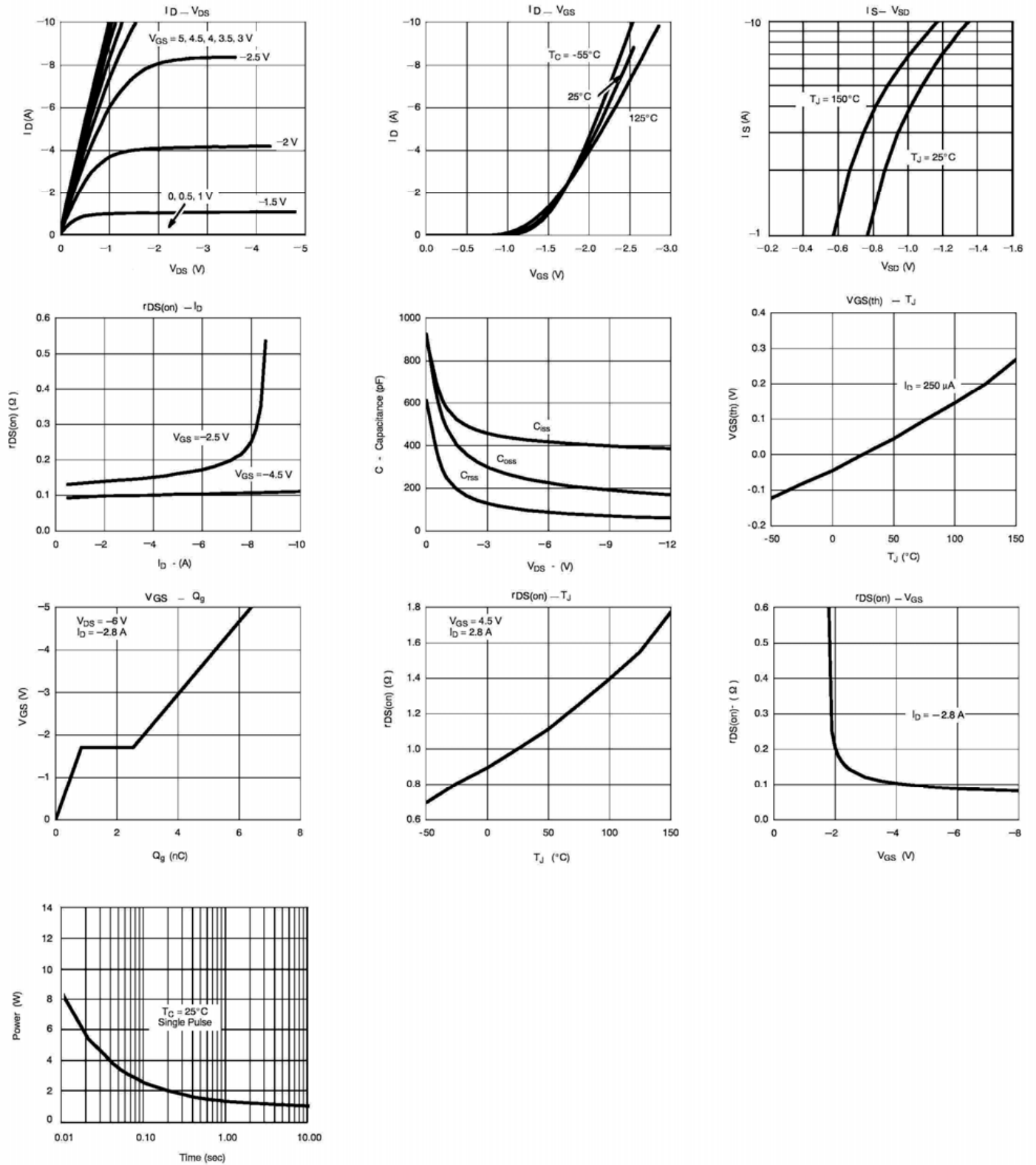
2. Guaranteed by design, not subject to production testing.



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## Dual P-Enhancement Field Effect Transistor

### Ratings and Characteristic Curves





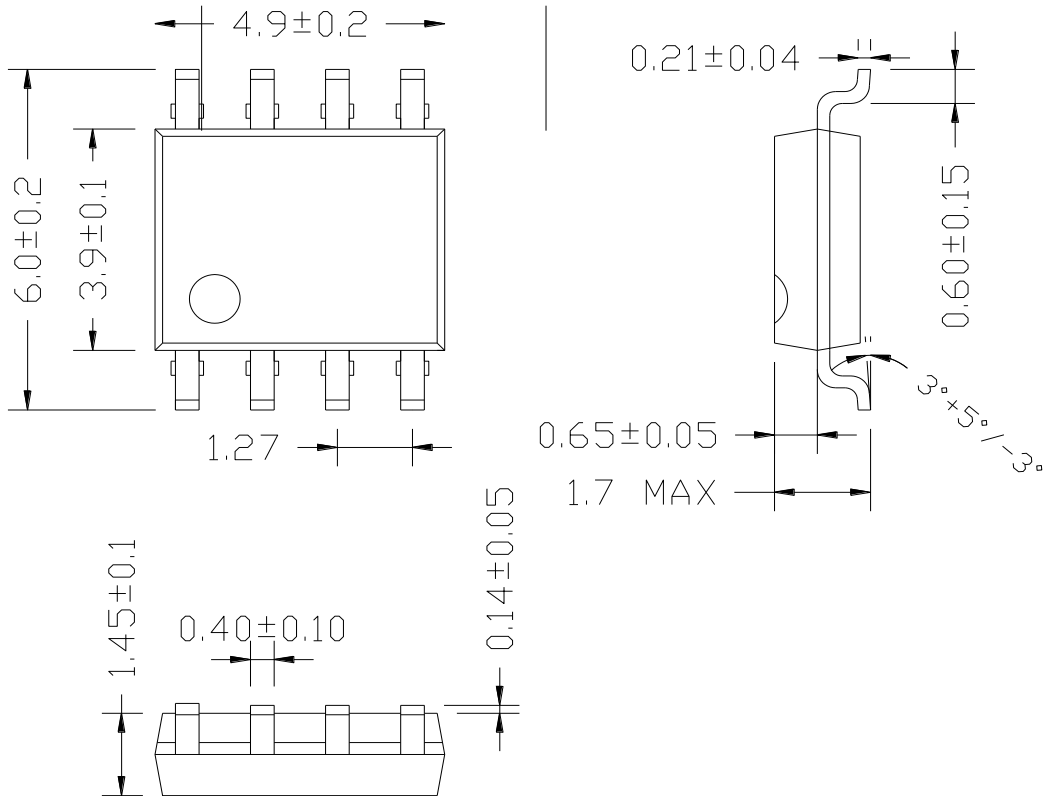
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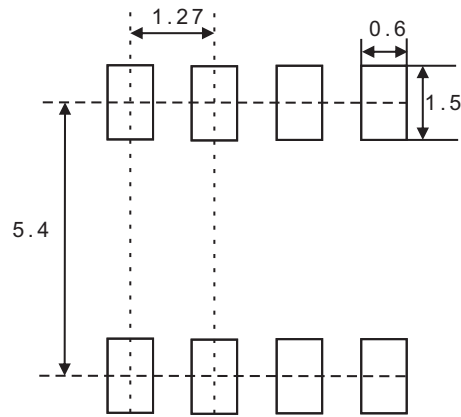
### Package Outline

SOP-8

unit: mm



### Recommended soldering pad



unit: mm

### Ordering Information

Device	Package	Shipping
PJM204A5DPPA	SOP-8	4,000PCS/T&R(13 inch)